IN THE CLAIMS

Claims 1-20 (Canceled)

21. (New) A semiconductor integrated circuit comprising:

a multiport memory which has a plurality of static RAMs;

a first circuit which receives first address signals and second address signals in parallel in synchronism with a first clock signal; and

a second circuit which supplies said first address signals and said second address signals to each of said static RAMs in serial in synchronism with a second clock signal higher than said first clock signal in frequency,

wherein said plurality of static RAMs are activated in parallel in synchronism with said second clock signal.

22. (New) A semiconductor integrated circuit according to claim 21,

wherein two or more cycles of said second clock signal are included in one cycle of said first clock signal,

wherein a read operation from said plurality of static RAMs is performed in a first cycle of said second clock signal, and

wherein a write operation to said plurality of static RAMs is performed in a second cycle subsequent to said first cycle.

23. (New) A semiconductor integrated circuit according to claim 21,

wherein two or more cycles of said second clock signal are included in one cycle of said first clock signal,

wherein a first write operation to said plurality of static RAMs is performed in a first cycle of said second clock signal, and

wherein a second write operation to said plurality of static RAMs is performed in a second cycle subsequent to said first cycle.